FIG. 1

FUNDAMENTAL CELL IN ACCORDANCE WITH THE PRESENT INVENTION

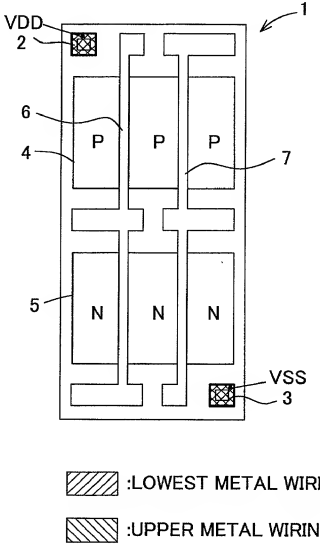


FIG. 2

FUNCTIONAL CIRCUIT BLOCK FORMED BY USING FUNDAMENTAL CELLS IN ACCORDANCE WITH THE PRESENT INVENTION

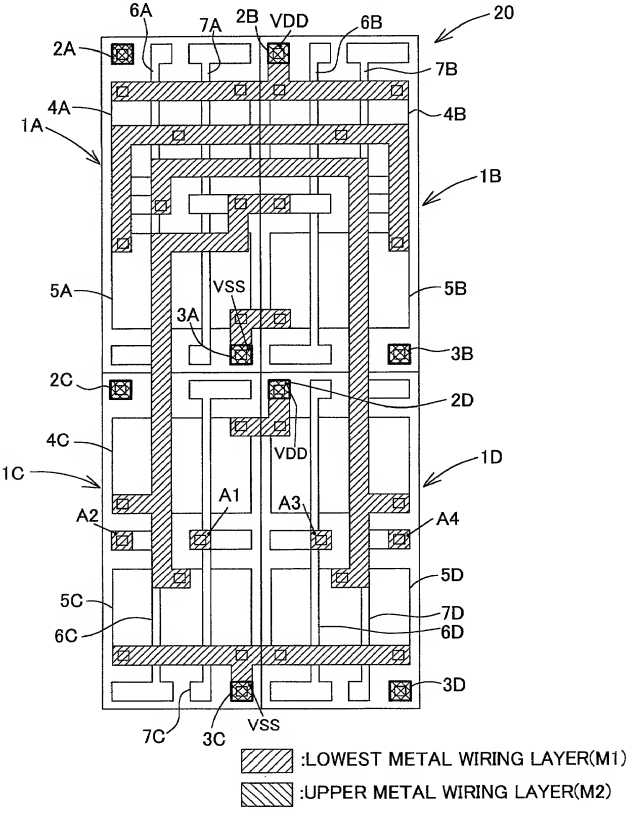
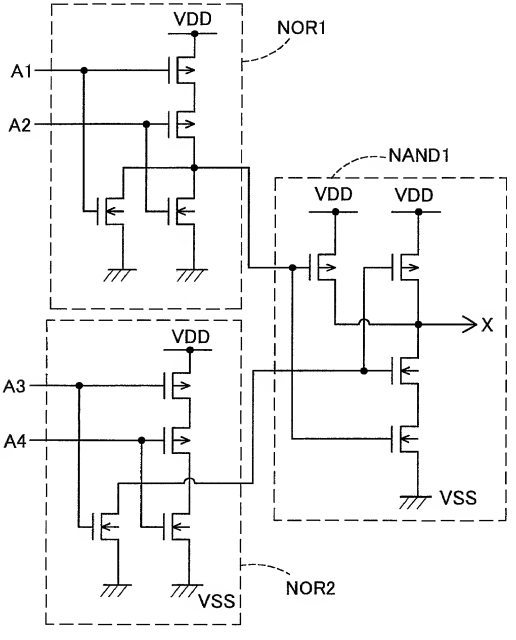


FIG. 3

CIRCUIT DIAGRAM OF THE FUNCTIONAL CIRCUIT BLOCK SHOWN IN FIG.2



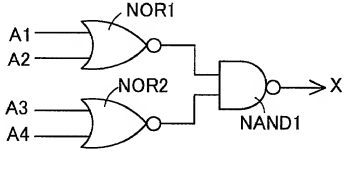


FIG. 4

FIRST PRACTICAL EMBODIMENT OF POWER RAILS WHEN THE FUNDAMENTAL CELLS IN ACCORDANCE WITH THE PRESENT INVENTION ARE ARRANGED IN A FORM OF MATRIX

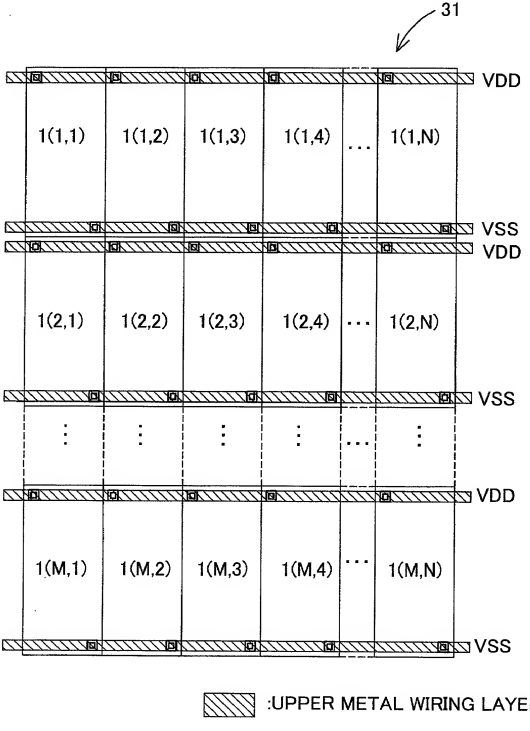


FIG. 5

SECOND PRACTICAL EMBODIMENT OF POWER RAILS WHEN THE FUNDAMENTAL CELLS IN ACCORDANCE WITH THE PRESENT INVENTION ARE ARRANGED IN A FORM OF MATRIX

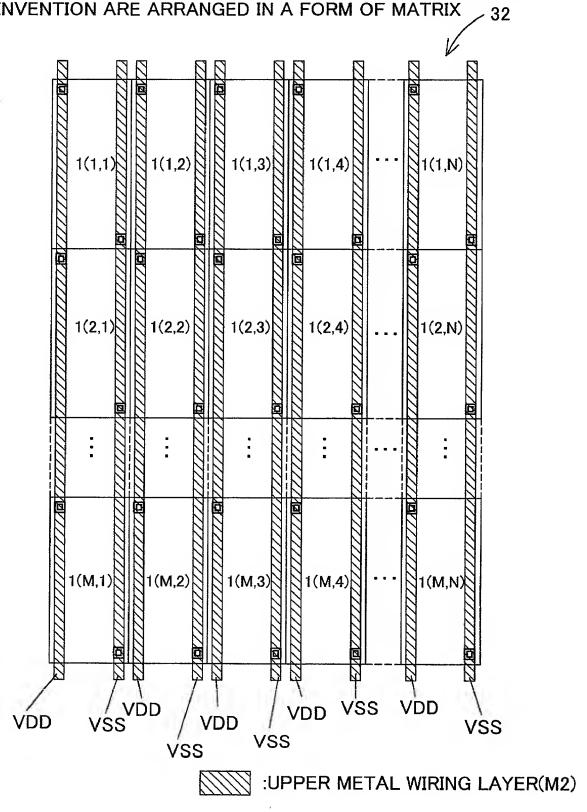


FIG. 6

THIRD PRACTICAL EMBODIMENT OF POWER RAILS WHEN THE FUNDAMENTAL CELLS IN ACCORDANCE WITH THE PRESENT INVENTION ARE ARRANGED IN A FORM OF MATRIX

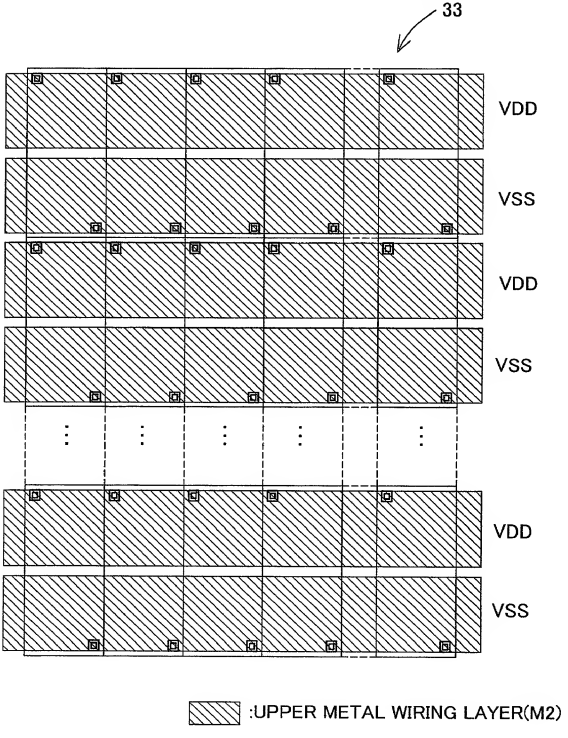


FIG. 7

FOURTH PRACTICAL EMBODIMENT OF POWER RAILS WHEN THE FUNDAMENTAL CELLS IN ACCORDANCE WITH THE PRESENT INVENTION ARE ARRANGED IN A FORM OF MATRIX

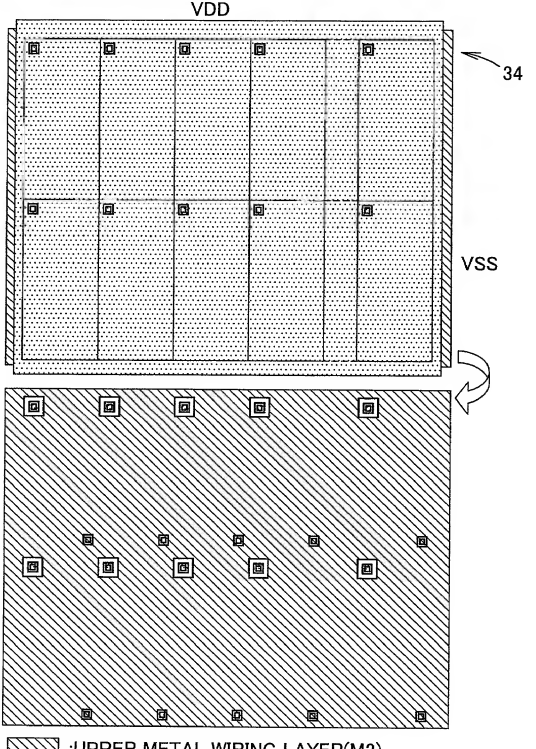


FIG. 8

FIFTH PRACTICAL EMBODIMENT OF POWER RAILS WHEN THE FUNDAMENTAL CELLS IN ACCORDANCE WITH THE PRESENT INVENTION ARE ARRANGED IN A FORM OF MATRIX

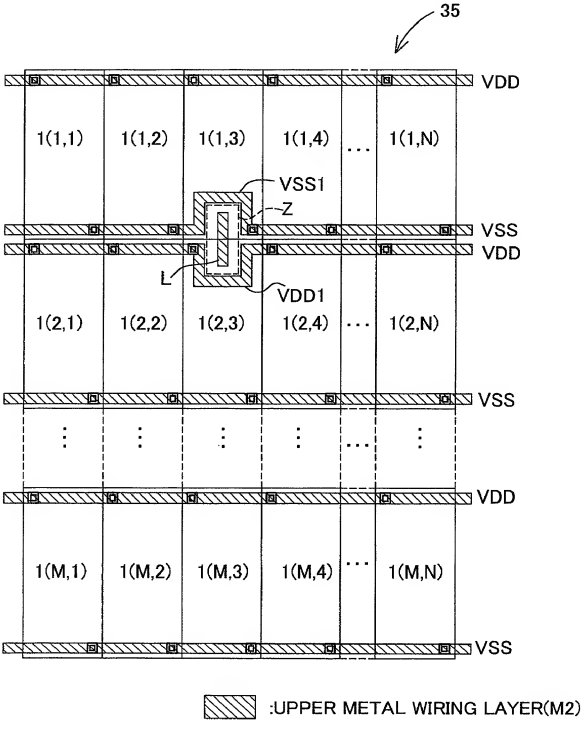


FIG. 9

SIXTH PRACTICAL EMBODIMENT OF POWER RAILS WHEN THE FUNCTIONAL CIRCUIT BLOCKS IN ACCORDANCE WITH THE PRESENT INVENTION ARE ARRANGED TO FORM A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

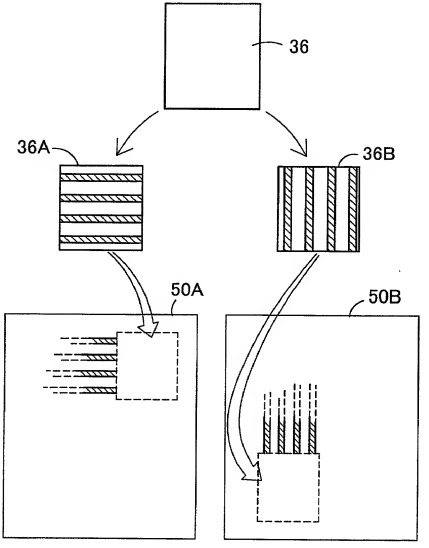


FIG. 10

BLOCK DIAGRAM OF A WIRING APPARATUS IN ACCORDANCE WITH THE PRESENT INVENTION

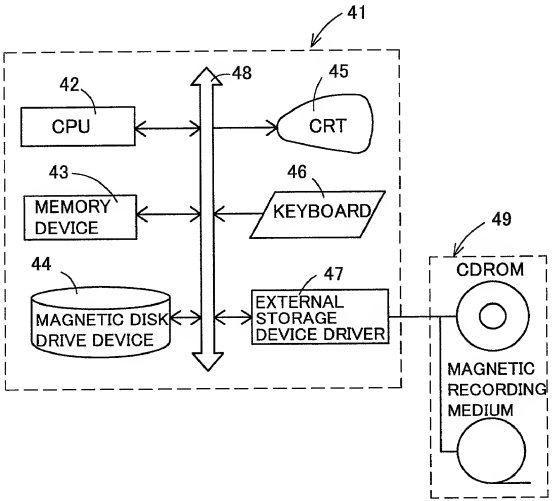


FIG. 11

A FLOW CHART OF A WIRING METHOD FOR WIRING IN A FUNCTIONAL CIRCUIT BLOCK USING THE FUNCTIONAL CIRCUIT BLOCKS IN ACCORDANCE WITH THE PRESENT INVENTION

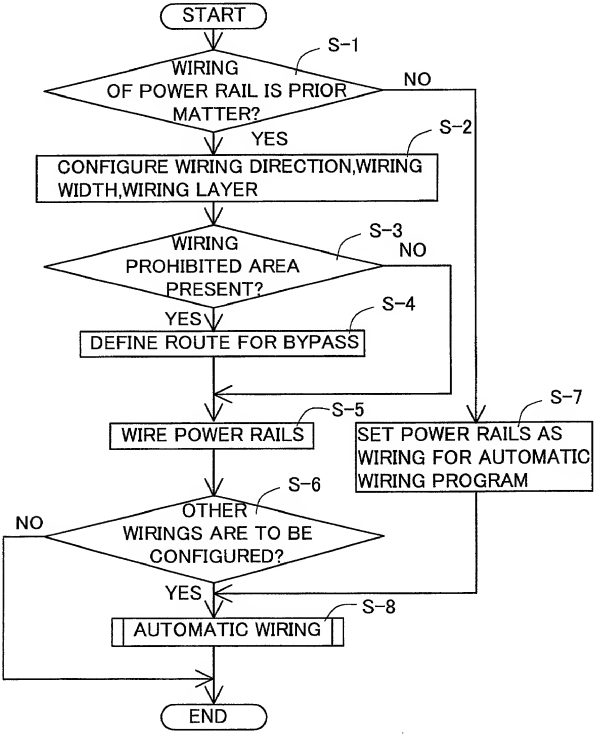
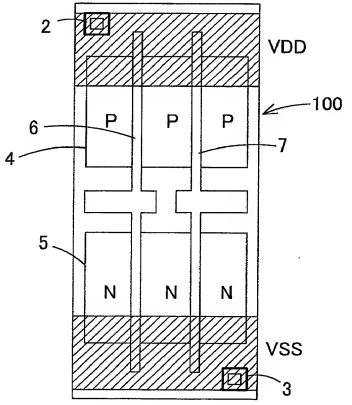


FIG. 12 PRIOR ART

FUNDAMENTAL CELL IN ACCORDANCE WITH THE RELATED ART



:LOWEST METAL WIRING LAYER(M1)

FIG. 13 PRIOR ART

FUNCTIONAL CIRCUIT BLOCK FORMED BY USING THE FUNDAMENTAL CELLS OF THE RELATED ART

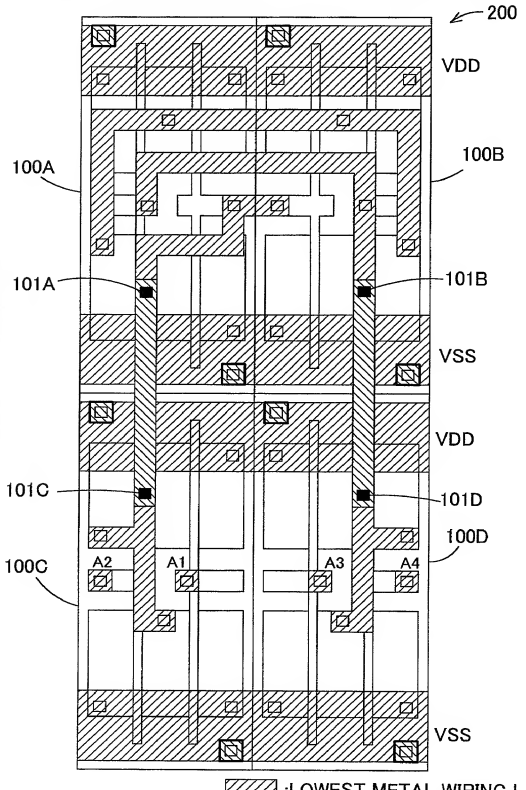


FIG. 14 PRIOR ART

POWER RAIL EMBODIMENT WHEN FORMING THE FUNDAMENTAL CELLS OF THE RELATED ART IN A FORM OF MATRIX